IN THE CLAIMS

Please amend claims 26 and 27 and insert new claim 41-46 as follows:

Claims 1-20. Cancelled

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21. (Previously Presented) A computer system, in which a part of main memory is able to be hot-plugged, said computer system comprising,

a first memory,

a non-volatile storage storing first memory information of said first memory size and a second memory information of a second memory to be hot-plugged,

a processor acquiring said first and second memory information from said non-volatile storage and mapping said first memory based on said first and second memory information.

22. (Previously Presented) A computer system according to claim 21,

wherein said processor generating first logical-physical address translating table for said first memory based on said first and second memory information and stores at least a part of said first logical-physical address translating table in said first memory, and

wherein said processor assigns a region to store a second logical-physical address translating table for said second memory in said first memory.

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23. (Previously Presented) A computer system according to claim 22,

wherein said first memory has a non-translatable region, and

wherein said processor uses said non-translatable region for said first and second logical-physical address translating table.

24. (Previously Presented) A computer system according to claim 22,

wherein said processor has TLB.

25. (Previously Presented) A computer system according to claim 21,

wherein said non-volatile storage is EEPROM.

26. (Currently Amended) A computer system comprising,

a first main memory,

a non-volatile storage storing a first configuration information of said first main memory and second configuration information of a second main memory to be hot-added, and

a processor acquiring said first and second configuration information ~~form~~ from said non-volatile storage on memory-mapping of said first main memory.

27. (Currently Amended) A computer system according to claim 26,

wherein said processor assigns a non-address translated region in said first main memory ~~on~~ when memory-mapping ~~of~~ said first main memory.

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28. (Previously Presented) A computer system according to claim 27,

wherein said processor determines size of said non-address translated region based on said first and second configuration information.

29. (Previously Presented) A computer system according to claim 28,

wherein said processor generates a first logical-physical address translation pairs of said first main memory based on said first configuration information and stores at least a part of said logical-physical address translation pairs in said non-address translated region.

30. (Previously Presented) A computer system according to claim 28,

wherein said processor assigns a region a second logical-physical address translating pairs of said main memory in said non-address translated region.

31. (Previously Presented) A computer system according to claim 26,

wherein said non-volatile storage is EEPROM.

32. (Previously Presented) A computer system according to claim 26,

wherein said processor has TLB.

33. (Previously Presented) A computer system, which supports a virtual memory system, said computer system comprising,

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a first main memory,

a non-volatile storage storing a first information setting a memory size of a second main memory to be hot-inserted,

a processor mapping said first main memory and acquiring said first information upon said mapping.

34. (Previously Presented) A computer system according to claim 33,

wherein said processor assigns a top priority region of interrupt handling in said first main memory.

35. (Previously Presented) A computer system according to claim 34,

wherein said processor acquires a memory size of said first main memory and determines said not priority region from said memory size of said first main memory and said first information.

36. (Previously Presented) A computer system according to claim 35,

wherein said processor generates a first logical-physical address translation pairs of said first main memory and stores at least a part of said first logical-physical address translating pairs in said top priority region.

37. (Previously Presented) A computer system according to claim 35,

wherein said processor reserves a region to store a second logical-physical address translation pairs of said second main memory in said top priority region.

38. (Previously Presented) A computer system according to claim 33,

wherein said non-volatile storage EEPROM.

39. (Previously Presented) A computer system according to claim 35,

wherein said processor has a logical-physical address translating unit.

40. (Previously Presented) A computer system according to claim 39,

wherein said processor has TLB.

41. (New) A computer system according to claim 21, wherein the non-volatile storage stores the second memory information preliminarily before the second memory is hot-plugged.

42. (New) A computer system according to claim 21, wherein the non-volatile storage stores the second memory information when the computer system is powered on.

43. (New) A computer system according to claim 26, wherein the non-volatile storage stores the second configuration information of the second main memory in advance of the hot-adding of the second main memory.

44. (New) A computer system according to claim 26, wherein the non-volatile storage stores the second

B1 configuration information of the second main memory when the computer system is powered on.

45. (New) A computer system according to claim 33, wherein the non-volatile storage stores the first information prior to the hot-insertion of the second main memory.

46. (New) A computer system according to claim 33, wherein the non-volatile storage stores the first information when the computer system is powered on.